SPECIFICATION

Please modify paragraph [0001] of the specification as follows:

[0001] This application is related to the following commonly owned and co-filed U.S. Patent applications, filed January 30, 2004 and incorporated herein by reference: ~~Method and program product for determining worst case currents in a digital integrated circuit through worst case superposition of partial currents (Attorney Docket No. 200300123-1); Systems and methods that identify equivalent instantiation specific configuration information for analysis tools (Attorney Docket No. 200308898-1); System and method for determining detail of analysis in a circuit design (Attorney Docket No. 200308899-1); System and method for indicating logic state combinations used during circuit design analysis (Attorney Docket No. 200308900-1); Systems and methods for re using circuit design analysis results (Attorney Docket No. 200308901-1); System and method for balancing run-time and result accuracy in a circuit design analysis tool (Attorney Docket No. 200310170-1); System and method for determining control signal combinations for use during simulation of a stage of a circuit design (Attorney Docket No. 200310171-1); and System and method to limit analyzed current flow in a circuit design (Attorney Docket No. 200310173-1)~~ U.S. Patent Application Number 10/769,675, titled "Method and program product for determining worst case currents in a digital integrated circuit through worst-case superposition of partial currents"; U.S. Patent Application Number 10/769,495, titled "Systems and methods that identify equivalent instantiation-specific configuration information for analysis tools"; U.S. Patent Application Number 10/769,687, titled "System and method for determining detail of analysis in a circuit design"; U.S. Patent Application Number 10/769,676, titled "System and method for indicating logic state combinations used during circuit design analysis"; U.S. Patent Application Number 10/769,702, titled "Systems and methods for re-using circuit design analysis results"; U.S. Patent Application Number 10/769,683, titled "System and method for balancing run-time and result accuracy in a circuit design analysis tool"; U.S. Patent Application Number 10/769,673, titled "System and method for determining control signal combinations for use during simulation of a stage of a circuit design"; and U.S. Patent Application Number 10/769,682, titled "System and method to limit analyzed current flow in a circuit design".

Please modify paragraph [0020] of the specification as follows:

[0020] Configuration tool 122 creates a hierarchical model 140 based upon circuit design 116 in computer memory 104. Hierarchical model 140 is illustratively shown with two

design elements 142 and 146. Design element 142 has a configuration element 144, and design element 146 has a configuration element 148. Design elements 142 and 146 are, for example, signal nets within circuit design 116. Capacitors, transistors and resistors may also be design elements.

Please modify paragraph [0025] of the specification as follows:

[0025] FIG. 2 shows one exemplary cell I0 that includes circuitry to provide inverter functionality. Cell I0 is, for example, suitable for use within circuit design 116, FIG. 1. Cell I0 has four ports 210, 212, 214 and 216 and, in this example, includes a p-type field-effect transistor ("FET") 204 and an n-type FET 206 connected serially between port 214 and port 216. Port 214, labeled 'V', connects to power rail Voltage-Drain-Drain (VDD) and port 216, labeled 'G', connects to ground rail (GND). Cell I0 also has four signal nets ~~220, 222,~~ IN, OUT, 224 and 226: signal net ~~220~~ IN connects port 210 to gate terminals of FETs 204 and 206; signal net ~~222~~ OUT connects a drain terminal of FET 204 and a source terminal of FET 206 (i.e., a common point between FETs 204 and 206) to output port 212; signal net 224 connects a source terminal of FET 204 to port 214; and signal net 226 connects a drain terminal of FET 206 to port 216. As shown in FIG. 3, cell I0 may be used within other cells to provide the inverter functionality, each use instantiating cell I0 within circuit design 116.

Please modify paragraph [0026] of the specification as follows:

[0026] FIG. 3 illustrates one exemplary cell 300 with two instantiations I1, I2 of cell I0, FIG. 2. Cell 300 is, for example, suitable for use in circuit design 116, FIG. 1. Cell 300 has four ports 302, 304, ~~306 and~~ 308 and 310. Port 302 is an input port that is connected to port 210(1) of cell instance I1 by signal net A. Port 212(1) of cell instance I1 is connected to port 210(2) of cell instance I2 by signal net B. Signal net C connects port 212(2) of cell instance I2 to output port 304. Port 308, labeled 'V', connects to power rail VDD and port 310, labeled 'G', connects to ground rail GND. Net 312 connects port 308 to ports 214(1) and 214(2); and net 314 connects port 310 to ports 216(1) and 216(2).